[54] **SEMICONDUCTOR MEMORY**

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[73] Assignee: Hitachi, Ltd., Tokyo, Japan

[*] Notice: The portion of the term of this patent subsequent to Oct. 25, 2005 has been disclaimed.

[21] Appl. No.: 288,314

[22] Filed: Oct. 11, 1988

Related U.S. Application Data

[62] Division of Ser. No. 873,072, Jun. 24, 1986, Pat. No. 4,799,192.

[30] **Foreign Application Priority Data**

Jun. 26, 1985 [JP] Japan 60-137733

[51] Int. Cl.* G11C 7/00

[52] U.S. Cl. 365/204; 365/205

[58] Field of Search 365/149, 103, 205, 208, 365/210

[56] **References Cited**

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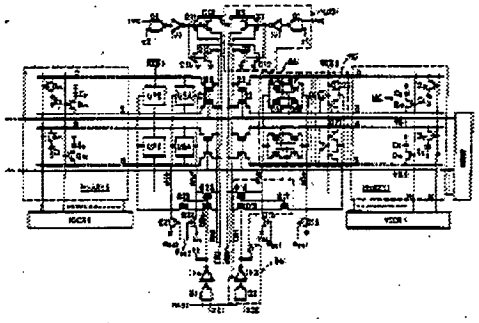
H. Kawamoto et al., "A 288 Kb CMOS Pseudo SRAM", 1984 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 276-277.

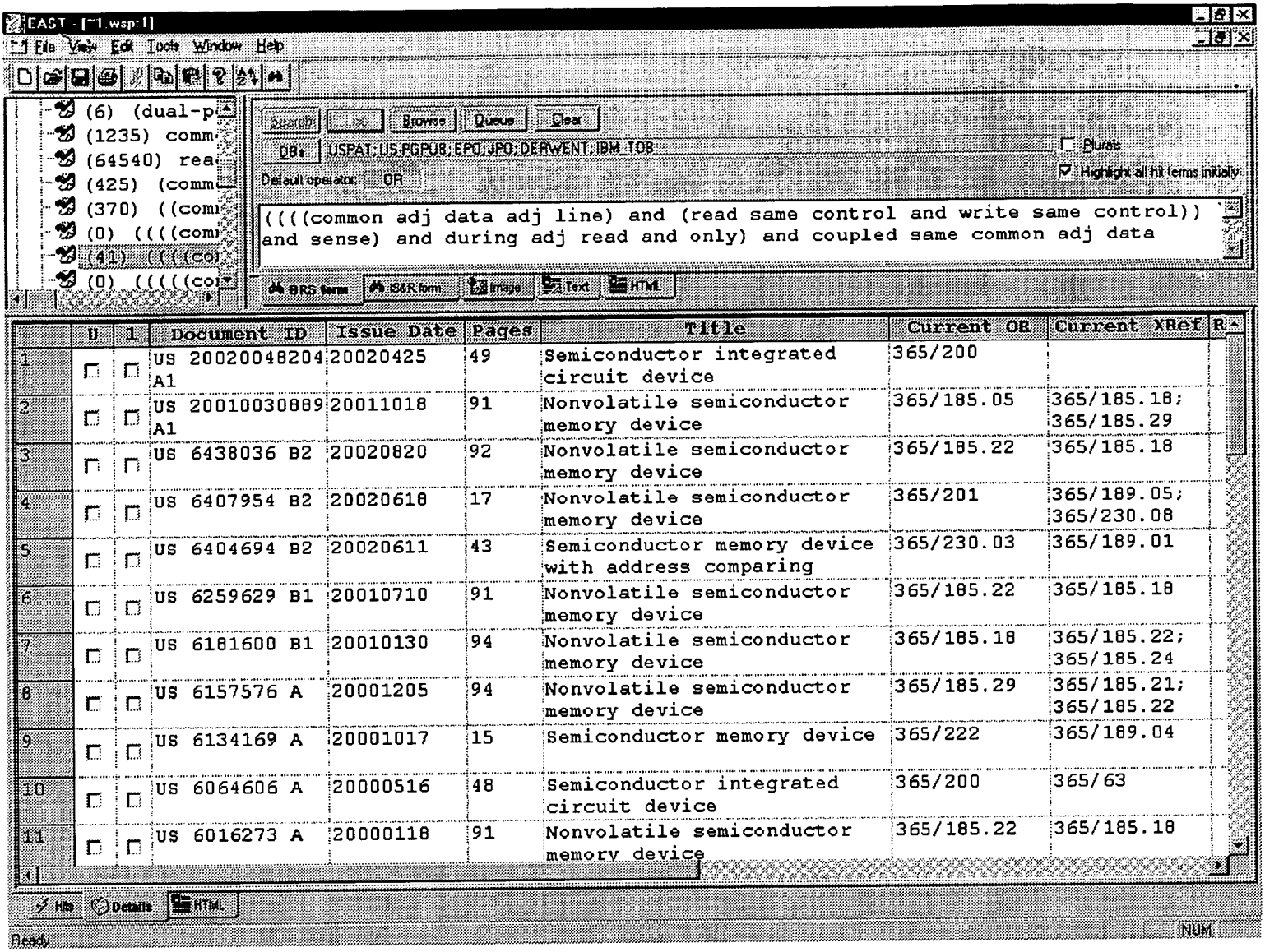
Primary Examiner—Joseph A. Popek
Attorney, Agent, or Firm—Antonelli, Terry & Wands

[57] **ABSTRACT**

A dynamic RAM is arranged such that a common data line in each of the non-selected ones of the divided memory arrays is connected to a pair of common source lines of a sense amplifier corresponding to the memory array concerned, whereby the potential of the common data line is set at a medium level which is substantially equal to the potential of the data lines by utilizing the medium potential of the pair of common source lines and a relatively large parasitic capacity thereof, thereby maintaining the data lines at the half-precharge level. The pair of common source lines are shorted to each other during the non-select period of the memory arrays, so that the common source lines have a medium level which is substantially equal to the half-precharge level of the data lines.

20 Claims, 8 Drawing Sheets





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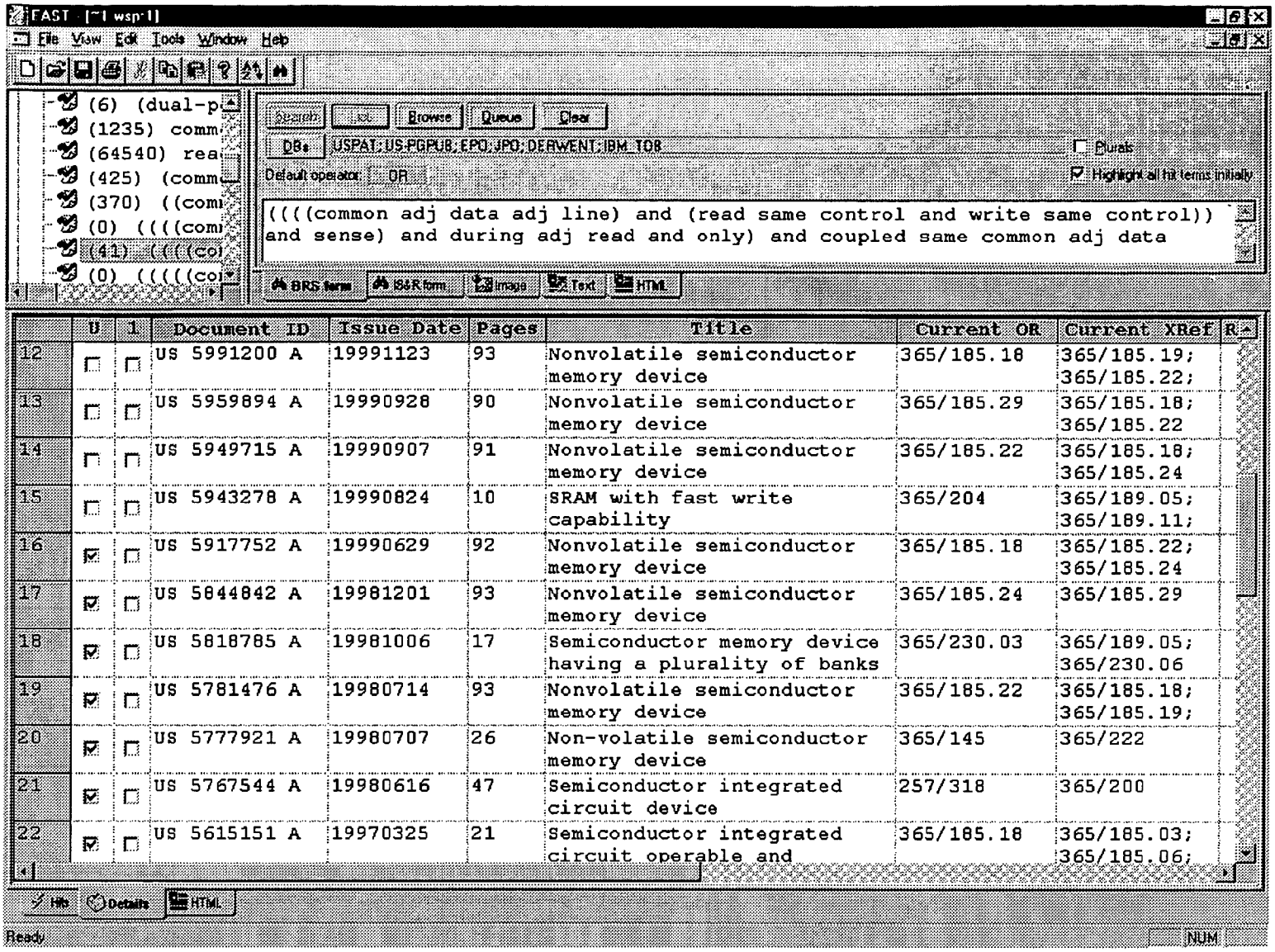
1	☐	☐	US 20020048204 A1	20020425	49	Semiconductor integrated circuit device	365/200		
2	☐	☐	US 20010030889 A1	20011018	91	Nonvolatile semiconductor memory device	365/185.05	365/185.18; 365/185.29	
3	☐	☐	US 6438036 B2	20020820	92	Nonvolatile semiconductor memory device	365/185.22	365/185.18	
4	☐	☐	US 6407954 B2	20020618	17	Nonvolatile semiconductor memory device	365/201	365/189.05; 365/230.08	
5	☐	☐	US 6404694 B2	20020611	43	Semiconductor memory device with address comparing	365/230.03	365/189.01	
6	☐	☐	US 6259629 B1	20010710	91	Nonvolatile semiconductor memory device	365/185.22	365/185.18	
7	☐	☐	US 6181600 B1	20010130	94	Nonvolatile semiconductor memory device	365/185.18	365/185.22; 365/185.24	
8	☐	☐	US 6157576 A	20001205	94	Nonvolatile semiconductor memory device	365/185.29	365/185.21; 365/185.22	
9	☐	☐	US 6134169 A	20001017	15	Semiconductor memory device	365/222	365/189.04	
10	☐	☐	US 6064606 A	20000516	48	Semiconductor integrated circuit device	365/200	365/63	
11	☐	☐	US 6016273 A	20000118	91	Nonvolatile semiconductor memory device	365/185.22	365/185.18	



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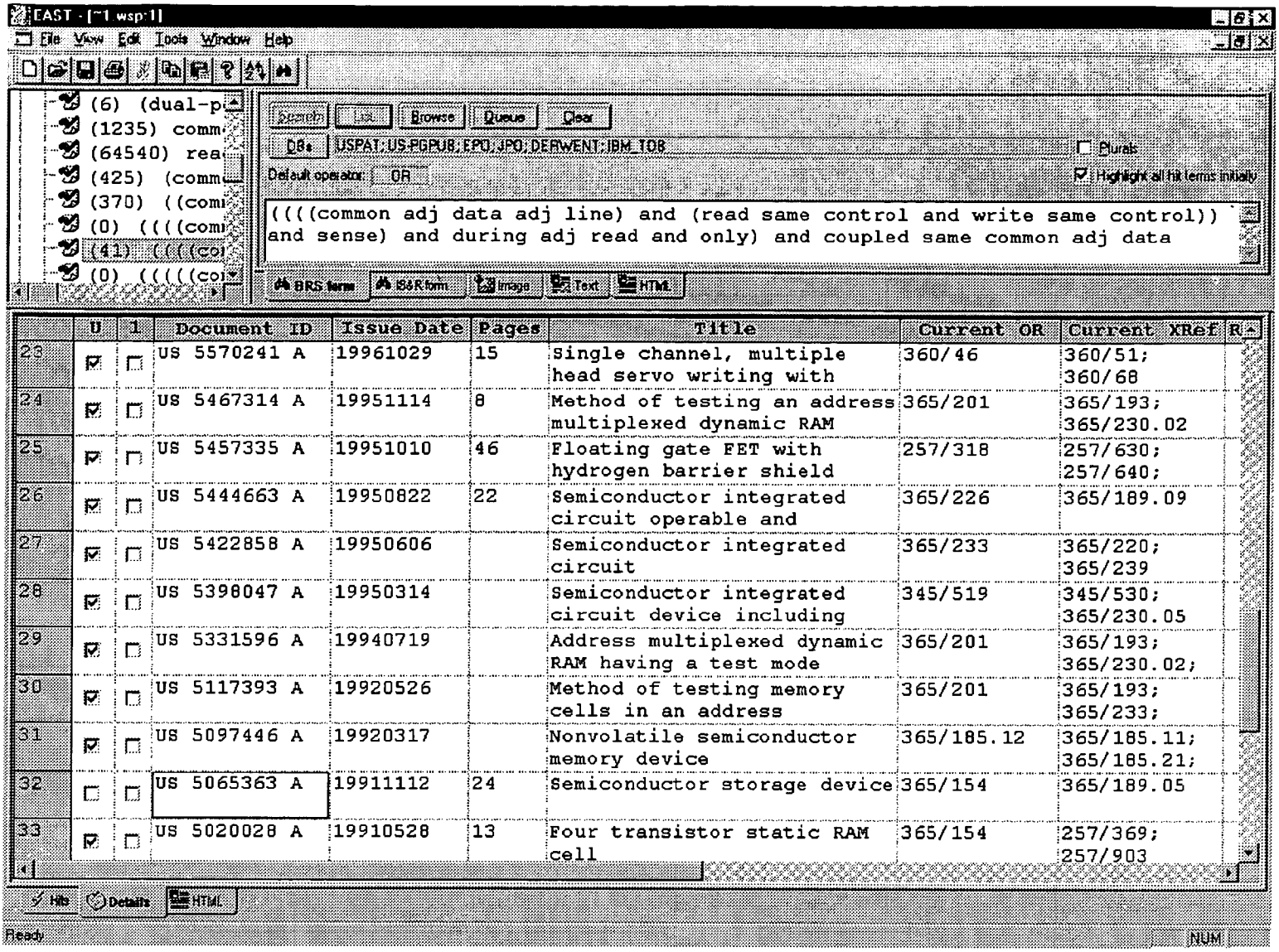
12	☐	☐	US 5991200 A	19991123	93	Nonvolatile semiconductor memory device	365/185.18	365/185.19; 365/185.22;	
13	☐	☐	US 5959894 A	19990928	90	Nonvolatile semiconductor memory device	365/185.29	365/185.18; 365/185.22	
14	☐	☐	US 5949715 A	19990907	91	Nonvolatile semiconductor memory device	365/185.22	365/185.18; 365/185.24	
15	☐	☐	US 5943278 A	19990824	10	SRAM with fast write capability	365/204	365/189.05; 365/189.11;	
16	☑	☐	US 5917752 A	19990629	92	Nonvolatile semiconductor memory device	365/185.18	365/185.22; 365/185.24	
17	☑	☐	US 5844842 A	19981201	93	Nonvolatile semiconductor memory device	365/185.24	365/185.29	
18	☑	☐	US 5818785 A	19981006	17	Semiconductor memory device having a plurality of banks	365/230.03	365/189.05; 365/230.06	
19	☑	☐	US 5781476 A	19980714	93	Nonvolatile semiconductor memory device	365/185.22	365/185.18; 365/185.19;	
20	☑	☐	US 5777921 A	19980707	26	Non-volatile semiconductor memory device	365/145	365/222	
21	☑	☐	US 5767544 A	19980616	47	Semiconductor integrated circuit device	257/318	365/200	
22	☑	☐	US 5615151 A	19970325	21	Semiconductor integrated circuit operable and	365/185.18	365/185.03; 365/185.06;	



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
23	☑	☐	US 5570241 A	19961029	15	Single channel, multiple head servo writing with	360/46	360/51; 360/68	
24	☑	☐	US 5467314 A	19951114	8	Method of testing an address multiplexed dynamic RAM	365/201	365/193; 365/230.02	
25	☑	☐	US 5457335 A	19951010	46	Floating gate FET with hydrogen barrier shield	257/318	257/630; 257/640;	
26	☑	☐	US 5444663 A	19950822	22	Semiconductor integrated circuit operable and	365/226	365/189.09	
27	☑	☐	US 5422858 A	19950606		Semiconductor integrated circuit	365/233	365/220; 365/239	
28	☑	☐	US 5398047 A	19950314		Semiconductor integrated circuit device including	345/519	345/530; 365/230.05	
29	☑	☐	US 5331596 A	19940719		Address multiplexed dynamic RAM having a test mode	365/201	365/193; 365/230.02;	
30	☑	☐	US 5117393 A	19920526		Method of testing memory cells in an address	365/201	365/193; 365/233;	
31	☑	☐	US 5097446 A	19920317		Nonvolatile semiconductor memory device	365/185.12	365/185.11; 365/185.21;	
32	☐	☐	US 5065363 A	19911112	24	Semiconductor storage device	365/154	365/189.05	
33	☑	☐	US 5020028 A	19910528	13	Four transistor static RAM cell	365/154	257/369; 257/903	

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the bit line capacitance charging operation. A write buffer operation, i.e., causing the capacitance component on a bit line to temporarily hold write charge information (high-speed bit line capacitance charging operation), can be performed at a relativ similar to a normal da respect to a DRAM (Dyn Access memory). For t information write oper to a memory cell trans within a short period write operation is vie the memory (EEPROM) (a of the second object).

Detailed Description Text - DETX (19):

FIG. 1 shows part of the arrangement of the EEPROM. An actual memory cell array includes many main/sub bit lines, word lines, selection gate lines, selection transistors, memory cell transistors, and the like. These memory cell transistors are arranged in the form of a matrix. Row and column decoder circuits (peripheral circuits) for specifying a predetermined memory cell in accordance with an external address input are connected to this memory cell matrix. A bit line precharge circuit and a sense amplifier for reading stored data from a specified memory cell transistor are connected to each of a

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L4: (18) sense adj am | US 5623444 | Tag: S | Doc: 15/18 | "Full" 1/26 (Tot...

United States Patent [19]

Gaten et al.

Patent Number: 5,623,444

Date of Patent: Apr. 22, 1997

[54] ELECTRICALLY-ERASABLE NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE HAVING A PULSE-DRIVEN MEMORY CELL TRANSISTOR

FOREIGN PATENT DOCUMENTS

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[57] ABSTRACT

37 Claims, 13 Drawing Sheets

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further comprises a shared p-sense amplifier, a shared n-sense amplifier, and a plurality of n-channel depletion transistors selectively coupling the plurality of pairs of digit lines to the shared p-sense amplifier and the n-sense amplifier .

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Detailed Description Text - DETX (3):

In the most general sense, a memory circuit comprises memory cells which store data. Depending upon the type of memory, this data can be read, or read and written. That is, some memories are read-only while others allow data to be read, manipulated, and re-written. Because many types of memories store data as a charge on a capacitor, sense amplifiers are implemented to detect small charges and amplify the charge for further processing. FIG. 1 is a simplified block diagram of a memory array 100 having memory cells 101 connected to a sense amplifier 102. The sense amplifier can be used to sense a charge stored on the memory cells and write the charge back to the memory

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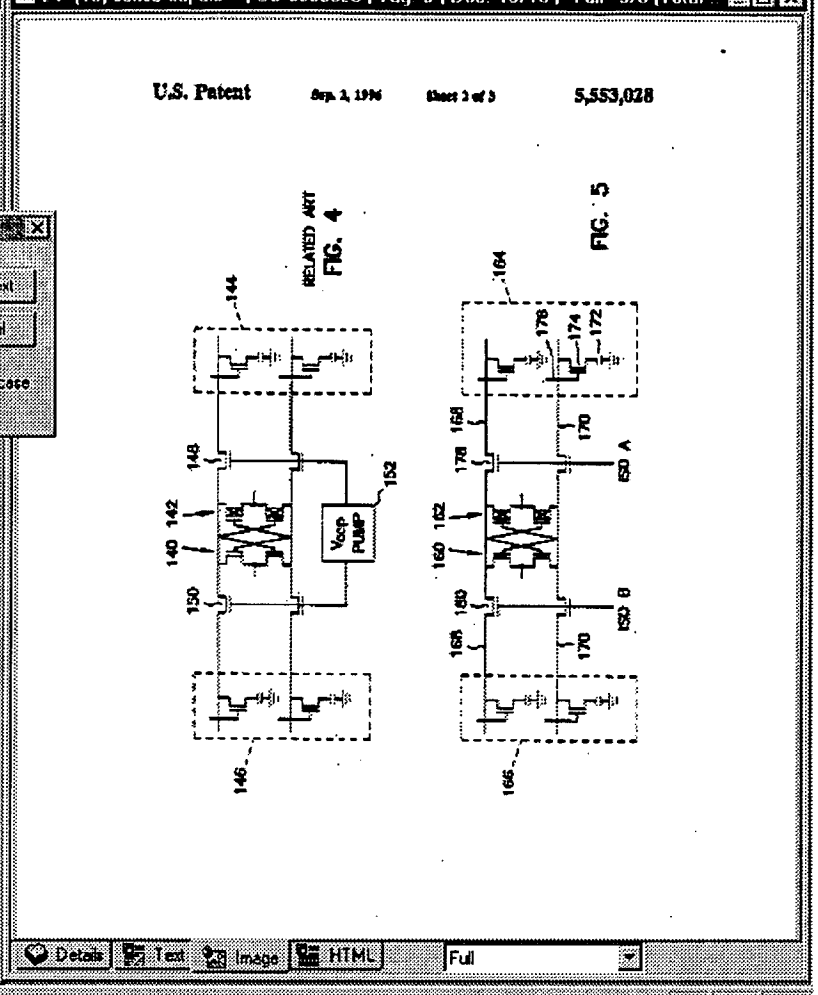

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[75] Inventors: Kazuhiko Kajigaya; Katsuyuki Sato, both of Kodaira, Japan

[73] Assignee: Hitachi, Ltd., Tokyo, Japan

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[51] Int. Cl.[4] G11C 7/00

[52] U.S. Cl. 365/203; 365/205

[58] Field of Search 365/149, 203, 205, 208, 365/210

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H. Kawamoto et al., "A 288 Kb CMOS Pseudo SRAM", 1984 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 276-277.

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18 Claims, 3 Drawing Sheets